DECODING SYSTEM AND METHOD

ABSTRACT

A cost-effective decoding apparatus that balances the flexibility of the software and performance of the hardware is presented. The decoder includes a bus, hardware modules connected to the bus and configured to execute a decoding process, and a processing unit connected to the bus, wherein the processing unit executes a decoding process by sending programmed signals to the hardware modules and responding to interrupts from the hardware components according to a set of programmed instructions. The instructions are re-programmable. As the hardware modules are configured to execute discrete tasks, the decoding process may be carried out in its entirety by sending signals to the hardware modules in the programmed order. Also presented is a method of decoding data by establishing communication with hardware modules that are each configured to execute a discrete task and activating the hardware modules in an order dictated by a computer program is also presented.